Amogh Somisetty

(925) 236-2600 | somisett@calpoly.edu | amogh.site | github.com/Asomisetty27 | linkedin.com/in/amoghsomisetty

Seeking a Summer 2027 engineering internship or a January to August 2027 co-op

Education

California Polytechnic State University, San Luis Obispo Expected June 2028
B.S. Electrical Engineering *San Luis Obispo, CA*

- **Coursework:** Computer Architecture, Digital Logic Design, Embedded Systems, Signals & Systems, Electronics (in progress)

Experience

Creator & Lead Researcher, Theta Mar 2026 – Present
Open-source GPU thermal-power forensics, advised by ex-Intel silicon-validation faculty *San Luis Obispo, CA*

- Blind-flagged 3 of **64 H100s** on **Princeton**'s Della cluster from telemetry alone, two invisible to temperature thresholds; the operator independently confirmed two, one replaced under RMA and one re-measured at **+47.8%** thermal resistance.
- Shipped the agent behind it (`pip install runtheta`): peer-relative thermal resistance ($R_\theta = \Delta T/P$) by two-way median polish across position- and power-matched NVML/DCGM peers, flagging degradation in **6 minutes** against a multi-day ticket loop.
- Found the method's own failure mode on a rented 8×A100 node, where baseboard position alone moves healthy R_θ by **52%** at matched power, and rebuilt the detector position-conditioned to recover all 3 flags at zero false positives.
- Authoring two manuscripts for peer-reviewed publication: a five-fleet failure taxonomy across ∼50,000 GPUs with a permutation null on every claim, and a detection-method paper.

Electrical Lead, Avionics & Power Apr 2026 – Present
Poly UAS, Cal Poly Unmanned Aerial Systems competition team *San Luis Obispo, CA*

- Own the aircraft's electrical system: designed a 48 V and DroneCAN backplane in KiCad (2-layer, 120×90 mm) that replaces a hand-wired harness on a 12S heavy-lift quad, **ERC and DRC clean**.
- Sized four independent 48 V pass-throughs to **14 A continuous and 30 A burst** per IPC-2221 on 2 oz copper, with dual-line CAN TVS, switchable 120 Ω terminations, and a written bring-up procedure.
- Now designing the team's **NVIDIA Jetson AGX Orin** carrier board and sensor modules (schematic capture and layout, in progress) to move the aircraft from ground-controlled flight to onboard real-time computer vision.

Optimization Engineering Intern, promoted from Lab Operations Intern Jun 2025 – Sep 2025
Natera, clinical genetic testing *Pleasanton, CA*

- Cut validation and packaging cycle time from ∼20 minutes to 10–12 (**over 40%**) on a high-throughput clinical line by mapping the workflow and eliminating redundant verification steps.

Technical Projects

RISC-V CPU (RV32I) on FPGA *SystemVerilog, Vivado, Basys-3*

- Implemented a multi-cycle full-ISA core from the RTL up (10-operation ALU, FSM control unit, 32×32 register file); closed timing through synthesis and place-and-route, tracing faults to the exact RTL by waveform debug.

Mixed-Signal DAC Signal Chain on a Custom PCB (with a lab partner) *AVR, LTspice, 2-layer OSH Park board*

- Simulated, fabricated, and bench-characterized a binary-weighted 4-bit DAC driven by register-level firmware, measuring **62.5 mV/step within ±1 LSB** across all 16 codes.

Pantry Shelf Vision (Justice Centered Edge AI) *YOLO11n, PyTorch, ONNX, Jetson Orin Nano*

- Built a 3-stage detection pipeline (SKU-110K pretrain, gap fine-tune, 15-frame on-site fine-tune) reaching **0.920 mAP50**, eliminating every false positive from a documented retail-to-site domain gap.
- Live-tested the full monitoring loop against a real camera before hardware bring-up, finding and fixing **4 defects**, including a monitor that reported total blindness as "all shelves OK."

Technical Skills

Hardware & EDA	KiCad (schematic capture, multilayer layout, fabrication), LTspice, IPC-2221 conductor sizing, power delivery and protection, board bring-up, oscilloscope, DMM, SMD/reflow soldering
Digital & Embedded	SystemVerilog RTL, Vivado (synthesis, place & route, static timing), FPGA bring-up (Artix-7), waveform debug, AVR and STM32 register-level firmware, CAN/DroneCAN, I2C, SPI, UART
Software & Systems	Python, C, Go, Bash, SQL, NVML, DCGM, Prometheus, SLURM, Kubernetes (Helm, client-go), Docker, Linux, Git, GitHub Actions CI, pytest, NumPy, pandas, scikit-learn

Leadership

Founder and President, Poly Engineering Consulting: lead client-facing engineering project teams Sep 2024 – Present

Lab Assistant, Cal Poly EPIC: taught embedded systems to precollegiate students Jun 2026 – Aug 2026